

CLAIMS

I claim:

- 1 1. An apparatus comprising:
2 a storage device to receive incoming data; and
3 a select circuit to select between a first strobe to strobe in the incoming data at a first
4 strobe rate and a second strobe to strobe in the incoming data at a second strobe rate.
- 1 2. The apparatus of claim 1, wherein the select circuit is a multiplexer.
- 1 3. The apparatus of claim 1, wherein the select circuit is to receive a select signal from a
2 value stored in a register.
- 1 4. The apparatus of claim 1 further including a register to store a programmable value used
2 to select between the first and second strobes.
- 1 5. The apparatus of claim 1, wherein the storage device is a first-in, first-out (FIFO) buffer
2 to receive incoming data to be buffered for transfer onto a data bus having different timing than
3 the first or second strobe rate.
- 1 6. The apparatus of claim 5, wherein the FIFO is comprised of latches to latch in the data
2 and output pairs of bits based on timing of the data bus.
- 1 7. The apparatus of claim 5, wherein the FIFO is comprised of four latches to strobe in four
2 bits of data and output a pair of bits onto the data bus during a first portion of a clock cycle and
3 another pair of bits during a second portion of the clock cycle.
- 1 8. The apparatus of claim 5 further including a second select circuit disposed in a data path
2 of the incoming data to introduce delay in the data path to maintain phase relationship between
3 the incoming data and the first or second strobe selected.
- 1 9. An integrated circuit comprising:
2 an interim first-in, first-out (FIFO) buffer to strobe in data from a memory based on a
3 first strobe signal or a second strobe signal, the strobe signals based on a configuration of the
4 memory to be used to store the data; and
5 a select circuit to select between the first strobe signal and the second strobe signal, the
6 first and second strobe signals to have different strobe rates to strobe in the data from the
7 memory.
- 1 10. The integrated circuit of claim 9, wherein the select circuit is a multiplexer.

1 11. The integrated circuit of claim 10, wherein the multiplexer is to receive a select signal
2 from a value stored in a register.

1 12. The integrated circuit of claim 10 further including a register to store a programmable
2 value to be used by the multiplexer to select between the first and second strobe signals.

1 13. The integrated circuit of claim 10, wherein the FIFO is comprised of latches to latch in
2 the data and output pairs of bits based onto an internal data bus based on timing of the data bus.

1 14. The integrated circuit of claim 10, wherein the FIFO is comprised of four latches to
2 strobe in four bits of data and output a pair of bits onto an internal data bus during a first portion
3 of a clock cycle and another pair of bits during a second portion of the clock cycle.

1 15. The integrated circuit of claim 10 further including a second multiplexer disposed in a
2 data path of the incoming data to introduce delay in the data path to maintain phase relationship
3 between the incoming data and the first or second strobe selected.

1 16. A method comprising:

2 generating a plurality of strobes;

3 selecting one strobe from the plurality of probes; and

4 receiving incoming data using the selected strobe.

1 17. The method of claim 16 further including multiplexing the plurality of strobes and using
2 a select signal for selecting the one strobe.

1 18. The method of claim 17 further including delaying the incoming data to maintain phase
2 relationship between the incoming data and the selected one strobe.

1 19. The method of claim 18, wherein the receiving incoming data includes latching in the
2 data and outputting pairs of bits based onto an internal data bus based on timing of the data bus.

1 20. The method of claim 18, wherein the receiving incoming data includes latching to strobe
2 in four bits of data and outputting a pair of bits onto an internal data bus during a first portion of
3 a clock cycle and another pair of bits during a second portion of the clock cycle.